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EXAMINER
MONDT, JOHANNES P

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 11/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/780,534	KONDO, KATSUFUMI	
	Examiner	Art Unit	
	Johannes P Mondt	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-5,7-10,13-16,18, 19 and 20 is/are rejected.

7)☒ Claim(s) 6,11,12, and 17 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2/17/04.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

The examiner has considered the items listed in the Information Disclosure Statement filed 02/17/2004. A signed copy of Form PTO-1449 is herewith enclosed.

Claim Objections

1. ***Claim 11*** is objected to because of the following informalities: the wording "great" (line 3) should be replaced by "greater" and the wording ", and the distance between the semiconductor light emitting layers is small near edges" (lines 4-6) should be replaced by "than the distance between the semiconductor light emitting layers near edges". Appropriate correction is required.

2. ***Claim 12*** is objected to because of the following informalities: the wording "small" (line 3) should be replaced by "smaller" and the wording ", and the distance between the semiconductor light emitting layers is great near edges" (lines 4-6) should be replaced by "than the distance between the semiconductor light emitting layers near edges". Appropriate correction is required.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. ***Claims 1, 3- 5, 8 and 9*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Ashida (Japanese Patent Application Publication with Publication Number 2001-068785 also published as Japanese Patent JP02002232005A; a computerized translation is attached to the Japanese original document and in addition Ashida (USPAT 6,567,449 B1 is available for translation to which reference is also made through column and line numbers when more convenient, and of which said Japanese Patent Application Publication is Foreign Priority) in view of Noto et al (Japanese Patent Application Publication with Publication Number 2002-232005, see computerized translation attached to the document while US Patent Application Publication US 2004/00611101 is available for translation).

Ashida teaches a semiconductor light emitting element (a laser is a specific kind of light emitting element) (cf. title) comprising (see USPAT to Ashida, col. 4, l. 38 – col. 6, l. 43):

a first layer 1/2/3 or, in an alternative, a first layer 1/2/3/4/5, (N.B.: a laminated layer is a specific kind of layer) (cf. English abstract);

a semiconductor light emitting layer 13 (cf. English abstract) selectively provided on the first layer (see front figure with abstract);

a current blocking layer 18 of high resistance provided around the semiconductor light emitting layer on the first layer (see section [0022] of computerized translation);

a second layer 15 (cf. section [0024] of computerized translation) provided on the semiconductor light emitting layer and the current blocking layer (see front figure with abstract);

a first electrode 19 (cf. section [0024] of computerized translation) provided on the second layer (see front figure with abstract);

a second electrode 10 (cf. section [0024] of computerized translation) provided on the back of the first layer (see front figure with abstract);

a part of the light emitted from the semiconductor light emitting layer being emitted outside is emitted (to the) outside at least either through the first layer or through the second layer because the laser beams of the two light-emitting sources in the invention by Ashida are aligned in the direction perpendicular to the substrate (cf. English abstract, "Problem to be Solved").

Ashida does not necessarily teach the limitation that a part of the light is emitted (to the) outside through both the first layer *and* the second layer.

However, it would have been obvious to include said limitation in view of Noto et al, who, in a patent application on a semiconductor laser with vertical emission and Group III / Group V active layer embodiments, - hence closely related to the invention by Ashida, teach that in order to improve light efficiency transparent (ITO = indium tin oxide) electrodes 8 and 10 (see English abstract) are included so as to allow light to be extracted in both upward and downward directions (cf. section [0010] o the computerized translation).

Motivation for inclusion of the teaching by Noto et al in this regard derives at least from the increased light extraction efficiency (see Noto et al, English abstract). *Combination* of said teaching with said invention is straightforward through electrode material selection as ITO bonds well with Group III – Group V semiconductor material.

On claim 3: the current blocking layer in Ashida is made of a semiconductor ($In_{0.49}$ $(Ga_{1-y}Al_y)_{0.51}P$ (y including the value y=0) with a bandgap that has a range overlapping with the range wherein said band gap is wider than a bandgap of the semiconductor light emitting layer ($Al_yGa_{1-y}As$) with preferable value y =0.1 (cf. sections [0019]-[0022] of the computerized translation), see, for instance, M. Levinstheyn et al, "Handbook Series on Semiconductor Parameters", World Scientific, Volumes 1 and 2, page 1, Volume 2, for the value 1.549 eV for the band gap of $Al_{0.1}Ga_{0.9}As$ and loc. cit., page 153 of Volume 2 for the value 1.811 eV for the band gap of $In_{0.49}Ga_{0.51}P$, given the values of the band gaps of InP (1.344 eV) (pages 169-170, Volume 1, loc.cit.) and GaP (2.26 eV) (pages 104-105, Volume 1, loc.cit.) (N.B.: Parenthetically, electrical resistivity as a property of the bulk of a body strongly and positively correlates with band gap while current blocking layers block the current because of their higher electrical resistivity in comparison with the active layer). In conclusion, the limitation is at least obvious because the compositional range that satisfies the limitation substantially overlaps the claimed range (i.e., the range defined by: band gap of blocking layer > band gap of light emitting layer). Furthermore, Applicant is reminded that it has been held that a *prima facie* case of obviousness typically exists when the ranges of a claimed composition overlap the ranges disclosed in the prior art or when the ranges of a claimed composition do not overlap but are close enough such that one skilled in the art would have expected them to have the same properties. In re Peterson, 65 USPQ2d 1379 (CA FC 2003).

On claim 4: the element by Ashida further comprises:

a first cladding layer 14 (see English abstract) provided between the first layer and the semiconductor light emitting layer and made of a semiconductor with band gap wider than the band gap of the semiconductor light emitting layer;

a second cladding layer 4 (see English abstract) provided between the first layer and the semiconductor light emitting layer and made of a semiconductor with band gap in a range ordained by a range in composition that includes a value for the band gap that is wider than the band gap of the semiconductor light emitting layer, because as we have seen above the band gap for the preferred value of y=0.1 of the light emitting layer is 1.549 eV while for instance for z=0.5 the value for the band gap of the second cladding layer of $In_{0.49}(Ga_{1-z}Al_z)P$ is approximately equal to 1.84 eV (M. Levinshteyn, loc.cit.);

wherein a refractive index of the current blocking layer is smaller than a refractive index of the light emitting layer, and the refractive index of the current blocking layer is greater than refractive indices of the first and second cladding layers, because the refractive index depends inversely on band gap (see for instance any text book, or, e.g., Ubukata (USPAT 6,434,178), col. 5, l. 13-15) while we have seen that the band gap of the current blocking layer is less than the band gap of both cladding layers while greater than that of the light emitting layer (see above, rejection of claims 1 and 3).

Parenthetically, the peculiar aspect to the limitation of claim 4, i.e., two cladding layers on the same side of the light-emitting layer, if not in (typographic?) error is indeed disclosed through cladding layers 2A and 2B (Figure 9 and its discussion of the first example) in Applicant's invention; whilst, in the unlikely event said claimed second

cladding layer was meant to be claimed as provided between the *second* layer and the semiconductor light emitting layer cladding layer 12 meets the claim (see English abstract).

On claim 5: in the element by Ashida at least one of the first and second layers has a slope on a side, namely: the second layer 15 (cf. front figure and discussion of ridge in computerized translation section [0018]).

On claim 8: a size (namely: its thickness) of the semiconductor light emitting layer is 20 μm or less, namely: 0.1 μm (col. 5, l. 35-38).

On claim 9: the element by Ashida further comprises conductive layer 9 provided between the first layer 1/3 and the second electrode 19 (see section [0019] and front figure). Although Ashida does not necessarily teach the further limitation that said conductive layer to be made of a material other than semiconductor material and allowing light emitted from the semiconductor light-emitting layer to pass through, it would have been obvious to include said further limitation in view of Noto et al, who, as discussed above, teach electrodes to be made of indium-tin-oxide, which is a transparent conductive oxide, not a semiconductor, so as to have the advantage of increasing light extraction efficiency. *Motivation* for inclusion of the teaching by Noto et al in this regard derives at least from the increased light extraction efficiency (see Noto et al, English abstract). *Combination* of said teaching with said invention is straightforward through electrode material selection as ITO bonds well with Group III – Group V semiconductor material.

3. ***Claim 7*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Ashida and Noto et al as applied to claim 1 above, and further in view of Kish et al US Patent Application Publication US 2003/0173571 A1). As detailed above, claim 1 is unpatentable over Ashida in view of Noto et al. But neither necessarily teach the further limitation as defined by this claim. However, it would have been obvious to include said further limitation in view of Kish et al, who, in a patent application on current blocking layer processing for active semiconductor devices including semiconductor lasers (title and abstract) teach semi-insulating current blocking layers through doping with superior oxygen content (abstract and sections [0017] and [0043]).

4. ***Claims 10, 14-16, 19 and 20*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Ashida (Japanese Patent Application Publication with Publication Number 2001-068785 also published as Japanese Patent JP02002232005A; a computerized translation is attached to the Japanese original document and in addition Ashida (USPAT 6,567,449 B1 is available for translation, of which said Japanese Patent Application Publication is Foreign Priority) in view of Noto et al (Japanese Patent Application Publication with Publication Number 2002-232005, see computerized translation attached to the document while US Patent Application Publication US 2004/00611101 is available for translation) and in view of Karpinski (USPAT 5,128,951).

On claim 10: Ashida teaches a semiconductor light emitting element (a laser is a specific kind of light emitting element) (cf. title) comprising:

a first layer 1/2/3, or, in an alternative a first layer 1/2/3/4 (N.B.: a laminated layer is a specific kind of layer) (cf. English abstract);

a semiconductor light emitting layer 13 (cf. English abstract) selectively provided on the first layer (see front figure with abstract);

a current blocking layer 18 of high resistance provided around the semiconductor light emitting layer on the first layer (see section [0022] of computerized translation);

a second layer 15 (cf. section [0024] of computerized translation) provided on the semiconductor light emitting layer and the current blocking layer (see front figure with abstract);

a first electrode 19 (cf. section [0024] of computerized translation) provided on the second layer (see front figure with abstract);

a second electrode 10 (cf. section [0024] of computerized translation) provided on the back of the first layer (see front figure with abstract);

a part of the light emitted from the semiconductor light emitting layer being emitted outside is emitted (to the) outside at least either through the first layer or through the second layer because the laser beams of the two light-emitting sources in the invention by Ashida are aligned in the direction perpendicular to the substrate (cf. English abstract, "Problem to be Solved").

Ashida does not necessarily teach the limitation that a part of the light is emitted (to the) outside through both the first layer *and* the second layer.

However, it would have been obvious to include said limitation in view of Noto et al, who, in a patent application on a semiconductor laser with vertical emission and

Group III / Group V active layer embodiments, - hence closely related to the invention by Ashida, teach that in order to improve light efficiency transparent (ITO = indium tin oxide) electrodes 8 and 10 (see English abstract) are included so as to allow light to be extracted in both upward and downward directions (cf. section [0010] o the computerized translation).

Motivation for inclusion of the teaching by Noto et al in this regard derives at least from the increased light extraction efficiency (see Noto et al, English abstract). *Combination* of said teaching with said invention is straightforward through electrode material selection as ITO bonds well with Group III – Group V semiconductor material.

Although Ashida does not specifically disclose an embodiment with a plurality of light emitting layers on the first layer being separated from each other in the sense of the Specification (Ashida does show two light emitting layers separated vertically rather than horizontally) it would at least have been obvious to include the limitation "*a plurality* of semiconductor light emitting layers selectively provided on the first layer, *the semiconductor light emitting layers being separated from each other* " *in view of Karpinski,* who, in a patent on a laser diode array teaches a plurality of semiconductor light emitting layers (the interface layers between the semiconductor layers forming the laser diode) on a single chip (abstract and col. 2, l. 50 – col. 3, l. 44) with vertical light emission. *Motivation* to include the teaching by Karpinski in the invention by Ashida derives at least clearly from the suggestion by Ashida (see [0025] in computerized translation or col. 6, l. 35-43 in USPAT 6,567,449) which, as mentioned can also serve as translation of Ashida, having Ashida as Foreign Priority) that his invention can be

extended to a plurality of light emitting regions for emission of multi-wavelength laser beams, as well as from Karpinski's motivation of obvious applications of laser arrays in a variety of fields (col. 1, l. 12-24). Because Ashida's invention when applied to laser arrays offers a simplification in the process of making (loc.cit.) combination of the teaching with the invention can reasonably expected to be successful.

On claim 14: the current blocking layer in Ashida is made of a semiconductor $(In_{0.49}(Ga_{1-y}Al_y)_{0.51}P$ (y including the value y=0) with a bandgap that has a range overlapping with the range wherein said band gap is wider than a bandgap of the semiconductor light emitting layer ($Al_yGa_{1-y}As$) with preferable value y =0.1 (cf. sections [0019]-[0022] of the computerized translation), see, for instance, M. Levinstheyn et al, "Handbook Series on Semiconductor Parameters", World Scientific, Volumes 1 and 2, page 1, Volume 2, for the value 1.549 eV for the band gap of $Al_{0.1}Ga_{0.9}As$ and loc. cit., page 153 of Volume 2 for the value 1.811 eV for the band gap of $In_{0.49}Ga_{0.51}P$, given the values of the band gaps of InP (1.344 eV) (pages 169-170, Volume 1, loc.cit.) and GaP (2.26 eV) (pages 104-105, Volume 1, loc.cit.) (N.B.: Parenthetically, electrical resistivity as a property of the bulk of a body strongly and positively correlates with band gap while current blocking layers block the current because of their higher electrical resistivity in comparison with the active layer). In conclusion, the limitation is at least obvious because the compositional range that satisfies the limitation substantially overlaps the claimed range (i.e., the range defined by: band gap of blocking layer > band gap of light emitting layer). Furthermore, Applicant is reminded that it has been held that a *prima facie* case of obviousness typically exists when the ranges of a claimed composition

overlap the ranges disclosed in the prior art or when the ranges of a claimed composition do not overlap but are close enough such that one skilled in the art would have expected them to have the same properties. In re Peterson, 65 USPQ2d 1379 (CA FC 2003).

On claim 15: the element by Ashida further comprises:

a first cladding layer 14 (see English abstract) provided between the first layer and the semiconductor light emitting layer and made of a semiconductor with band gap wider than the band gap of the semiconductor light emitting layer;

a second cladding layer 12 (see English abstract) provided between the first layer and the semiconductor light emitting layer and made of a semiconductor with band gap wider than the band gap of the semiconductor light emitting layer;

wherein a refractive index of the current blocking layer is smaller than a refractive index of the light emitting layer, and the refractive index of the current blocking layer is greater than refractive indices of the first and second cladding layers, because the refractive index inherently depends inversely on band gap (see for instance any text book, or, e.g., Ubukata (USPAT 6,434,178), col. 5, l. 13-15) while we have seen that the band gap of the current blocking layer is less than the band gap of both cladding layers while greater than that of the light emitting layer (see above, the rejection of claims 10 and 14).

On claim 16: in the element by Ashida at least one of the first and second layers has a slope on a side, namely: the second layer 15 (cf. front figure and discussion of ridge in computerized translation section [0018]).

On claim 19: a size (namely: its thickness) of the semiconductor light emitting layer is 20 μm or less, namely: 0.1 μm (col. 5, l. 35-38).

On claim 20: the element by Ashida further comprises conductive layer 9 provided between the first layer 1/3 and the second electrode 19 (see section [0019] and front figure). *Although Ashida does not necessarily teach* the further limitation that said conductive layer to be made of a material other than semiconductor material and allowing light emitted from the semiconductor light-emitting layer to pass through, it would have been obvious to include said further limitation in view of Noto et al, who, as discussed above, teach electrodes to be made of indium-tin-oxide, which is a transparent conductive oxide, not a semiconductor, so as to have the advantage of increasing light extraction efficiency. *Motivation* for inclusion of the teaching by Noto et al in this regard derives at least from the increased light extraction efficiency (see Noto et al, English abstract). *Combination* of said teaching with said invention is straightforward through electrode material selection as ITO bonds well with Group III – Group V semiconductor material.

5. ***Claim 2*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Ashida and Noto et al as applied to claim 1 above, and further in view of Fujimoto et al (6,242,761 B1). As detailed above, claim 1 is unpatentable over Ashida in view of Noto et al, neither of whom, however, necessarily teach the further limitation as defined by claim 2. However, it would have been obvious to include said further limitation in view of Fujimoto et al, who, in a patent to a Group II – Group V semiconductor light emitting

device, - hence closely related to the invention by Ashida, teach in an alternative within embodiment eight (cols. 20-21 and Figure 9) that the current blocking layer 907 (col. 20, l. 50) can be made in the light emitting layer 905 (col. 20, l. 49) itself by adding oxygen impurities ("oxidizing" is just that from an electrical viewpoint) to part of the light-emitting layer (cf. col. 21, l. 25-32). *Motivation* to include the teaching by Fujimoto in this regard in the invention by Ashida is derived from the advantage that the wafer can be removed when growth progresses to the light emitting layer (col. 21, l. 25-32), thus simplifying the process of making. Because *combination* of said teaching with said invention actually simplifies the process of making as explained above, *expectation of success* in implementing the combination can *reasonably be expected.*

6. ***Claim 13*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Ashida, Noto et al and Karpinski as applied to claim 10 above, and further in view of Fujimoto et al (6,242,761 B1). As detailed above, claim 10 is unpatentable over Ashida in view of Noto et al and Karpinski, none of whom, however, necessarily teach the further limitation as defined by claim 13. However, it would have been obvious to include said further limitation in view of Fujimoto et al, who, in a patent to a Group II – Group V semiconductor light emitting device, - hence closely related to the invention by Ashida, teach in an alternative within embodiment eight (cols. 20-21 and Figure 9) that the current blocking layers 907 (col. 20, l. 50) can be made in the light emitting layer 905 (col. 20, l. 49) itself by adding oxygen impurities ("oxidizing" is just that from an electrical viewpoint) to part of the light-emitting layers (cf. col. 21, l. 25-32). *Motivation* to include the teaching by Fujimoto in this regard in the invention by Ashida is derived from the

advantage that the wafer can be removed when growth progresses to the light emitting layers (col. 21, l. 25-32), thus simplifying the process of making. Because *combination* of said teaching with said invention actually simplifies the process of making as explained above, *expectation of success* in implementing the combination can *reasonably be expected.*

7. ***Claim 18*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Ashida and Noto et al as applied to claim 1 above, and further in view of Kish et al US Patent Application Publication US 2003/0173571 A1). As detailed above, claim 1 is unpatentable over Ashida in view of Noto et al, but neither necessarily teach the further limitation as defined by this claim. However, it would have been obvious to include said further limitation in view of Kish et al, who, in a patent application on current blocking layer processing for active semiconductor devices including semiconductor lasers (title and abstract) teach semi-insulating current blocking layers through doping with superior oxygen content (abstract and sections [0017] and [0043]).

Allowable Subject Matter

8. ***Claims 6, 11-12 and 17*** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. The following is a statement of reasons for the indication of allowable subject matter:

With regard to claims 6 and 17, and strictly within the context of the invention as defined by the respective independent claims 1 and 10, Ashida does not teach one of

first and second layers made of GaP in conjunction with semiconductor light emitting layers including InGaAlP, the light emitting layer meeting the claim being the upper light emitting layer in view of the limitations on current blocking layer; nor has prior art been found teaching all limitations of either claim 6 or 17 or over which the further limitation of either claim 6 or claim 17 is obvious in the sense of 35 USC 103(a);

With regard to claims 11-12: subject to meeting the conditions for removing the objections made above, and strictly within the context of the invention as defined by the respective independent claim 10, Ashida does not teach the distance between the semiconductor light emitting layers near the center to be either greater or smaller than near edges of the semiconductor light emitting element, merely having a suggestion on plurality of light emitting layers as claimed, whilst Karpinski does not teach the further limitation of either claim 11 or claim 12 either; nor has prior art been found teaching all limitations of claims 11 or 12 over which the further limitation of either claim 11 or claim 12 is obvious in the sense of 35 USC 103(a).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JPM
November 1, 2003

Patent Examiner:

Johannes Mondt
(Art Unit: 2826)